Remarks

Applicants thank the Examiner for his careful consideration of this application. Reconsideration of this application is now respectfully requested in view of the amendments above and the following remarks.

Claims 1-5, 7-14, 26-33, 35, 36, and 38-41 are now pending in the application, with Claims 1, 9, 26, 35, and 38 being the independent claims. Claim 6 has been cancelled without prejudice to pursue its subject matter subsequently. Claims 1, 9, 38, and 41 have been amended.

Applicants gratefully acknowledge the indication of allowable subject matter in Claims 9-13 at Page 4 of the Office Action. Claim 9 has been amended to incorporate the subject matter of Claim 1 and is now independent. It is respectfully submitted that Claims 9-13 are now in condition for allowance, and indication of such allowance is requested.

At Pages 2-5, the Office Action rejects Claims 1-3, 5, 6, 8, 26-29, 31, 33, 38, and 39 under 35 U.S.C. § 102(e) as being anticipated by Iwata et al. (U.S. Patent No. 6,876,055). Applicants respectfully traverse these rejections and/or respectfully submit that they are now moot based on the above amendments.

While Applicants do not intend to indicate agreement with the characterizations of the rejected claims and of the prior art reference used in their rejections, for the sake of expedience, they have opted to amend Claims 1, 38, and 41, as indicated above (Claim 41 is being mentioned here for convenience, even though it has not been rejected under the same grounds as Claims 1

and 38). In particular, each of these claims has been amended to recite that the claimed resistance region "has a non-zero impurity concentration lower than an impurity concentration of the [claimed] layer." As discussed in the Office Action, for example, at Page 3, and in the cited portions of Iwata et al. (col. 21, various lines), Iwata et al. uses an oxide resistance region, which is not doped with any impurities. In contrast, the present claim positively recites a resistance region containing impurities (i.e., "a non-zero impurity concentration"). Therefore, it is respectfully submitted that Iwata et al. fails to disclose at least this element of these claims, and for at least this reason, Claims 1-5, 7, 8, 14, and 38-41 are allowable over the cited prior art.

In connection with Claims 26-29, 31, and 33, it is noted that Claim 26, the independent claim from which the other rejected claims depend, includes, among other recitations, "a layer of a first conductivity type formed directly on a semiconductor substrate" and "a resistance region disposed in the layer between the first transistor and the body contact region." The Office Action, at Page 4, cites Fig. 17 and its description in Iwata et al. (cols. 22-23) as disclosing all of the elements of Claim 26, including these. Applicants note that the Office Action specifically cites the resistance region 316 as corresponding to the claimed resistance region. However, a careful review of Fig. 17 reveals that region 316 is not disposed in a layer of a first conductivity type, as claimed. On the contrary, region 316 forms a boundary between layers of two different conductivity types and thus can not correspond to the claimed resistance region.

Furthermore, at Page 4, the Office Action characterizes the term "substrate" as merely being a label, thus justifying the Office Action's characterization of element 312 of Fig. 17 as being the substrate on which the layer is formed. Applicants disagree with this characterization

of "substrate" and refer to col. 2 of Iwata et al. As discussed at col. 2, line 8, element 312 is an "N-type deep well region" and is formed on "a P-type semiconductor substrate 311," discussed at col. 2, line 7. As described at col. 2, lines 28-59, if there is no P-type substrate formed under the deep well regions, the device will not function properly. Therefore, the deep well regions, e.g., 312, are not the substrate; they are formed on the substrate.

For at least these reasons, it is respectfully submitted that Claims 26-33 are allowable over the cited prior art.

At Page 6, the Office Action rejects Claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. Applicants respectfully submit that Claim 4 is allowable over Iwata et al. for at least the reasons cited above in connection with Claims 1 et al. Furthermore, while Applicants do not necessarily concur with the Office Action's characterizations of the claim and of the prior art, Applicants choose not to provide further discussion at this time.

At Pages 6-7, the Office Action rejects Claims 7 and 32 under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. in view of Yamaguchi et al. (U.S. Patent No. 6,867,106). Applicants respectfully submit that these claims are allowable over the cited prior art for at least the reasons cited above. Applicants further respectfully traverse these rejections for the following reasons.

Claims 7 and 32 both recite "a discrete capacitor coupled between a body and a source of the first transistor." The Office Action cites Yamaguchi et al. at Fig. 3 and col. 8, lines 21-26. However, a careful review of the cited portions of Yamaguchi et al. reveals a discrete capacitor coupled between a body and a *gate* of a transistor, not between a body and a source. For this

further reason, it is respectfully submitted that Claims 7 and 32 are allowable over the cited prior art.

Finally, at Page 7, the Office Action rejects Claims 14, 30, 35, 36, 40, and 41 under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. in view of Wong et al. (U.S. Patent No. 6,246,094). These rejections are respectfully traversed for the following reasons.

Each of these claims either recites or depends from a claim that recites that a claimed layer is an epitaxial layer. The Office Action cites Wong et al. at Fig. 2D, layer 14, and col. 4, line 67 to col. 5, line 1 as teaching the use of such an epitaxial layer. However, the Office Action further recites that the motivation for using such an epitaxial layer is "for the purpose of preventing latch up in a CMOS integrated circuit," citing col. 1, lines 10-12. However, nowhere in Wong et al. is it taught that the use of an epitaxial layer is to prevent latch-up, nor is it true that the mere use of an epitaxial layer can prevent latch-up. (As a side note, Wong et al. teaches in the cited portions that "a buried shallow trench isolation structure" is used to prevent latch-up. Hence, it is the structure, not whether or not a layer is an epitaxial layer, that prevents latch-up in Wong et al.) Therefore, it is respectfully submitted that these rejections lack a motivation to combine the references and, therefore, do not constitute proper rejections of these claims.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants, therefore, respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

Date: June 8, 2005

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